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Multi-level parallel clocking of CCDs for: improving charge transfer efficiency, clearing persistence, clocked anti-blooming and generating low noise backgrounds for pumping

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ABSTRACT

A multi-level clocking scheme has been developed to improve the parallel CTE of four-phase CCDs by suppressing the effects of traps located in the transport channel under barrier phases by inverting one of these phases throughout the transfer sequence.

In parallel it was apparent that persistence following optical overload in Euclid VIS detectors would lead to undesirable signal released in subsequent rows and frames and that a suitable scheme for flushing this signal would be required. With care, the negatively biased electrodes during the multi-level transfer sequence can be made to pin the entire surface, row-by-row, and annihilate the problematic charges.

This process can also be extended for use during integration to significantly reduce the unusable area of the detector, as per the clocked anti-blooming techniques developed many years ago; however, with the four-phase electrodes architecture of modern CCDs, we can take precautionary measures to avoid the problem of charge pumping and clock induced charge within the science frames.

Clock induced charge is not all bad! We also propose the use of on-orbit trap-pumping for Euclid VIS to provide calibration input to ground based correction algorithms and as such a uniform, low noise background is required. Clock induced charge can be manipulated to provide a very suitable, low signal and noise background to the imaging array.

Here we describe and present results of multi-level parallel clocking schemes for use in four-phase CCDs that could improve performance of high precision astronomy applications such as Euclid VIS.

Keywords: CCD, CAB, CIC, BFW, SFW, tri-level, multi-level, Euclid VIS, CTE, persistence, blooming

1. INTRODUCTION

During the pre-development study phase for Euclid VIS [1], particular focus was given to optimising the parallel charge transfer efficiency (CTE) of the CCD273s [2] that comprise the focal plane and develop strategies to mitigate the reduced performance as a consequence of radiation damage during the mission [3]. Multiple electrode potential level parallel clocking schemes were investigated to: improve parallel CTE, eliminate surface persistence following optical overload and allow for Clocked Anti-Blooming (CAB) whilst avoiding Clock-Induced-Charge (CIC) and the ‘pumping’ of traps. With a greater understanding of CIC, a simple technique was developed to generate low noise charge injection via CIC for background generation used for trap pumping.

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2. MULTI-LEVEL PARALLEL CLOCKING

An example of a multiple level parallel clocking scheme is shown in Figure 1. In this example, three levels are used: +9 V, 0 V and -5 V. A commercial CCD camera electronics rack, supplied by XCAM Ltd., was adapted using four high speed differential amplifiers, each taking inputs from both image and store clock signals to provide the multiple level clock states. The adapter board and CCD loaded parallel clock waveforms during multiple line transfer are shown in Figure 2.

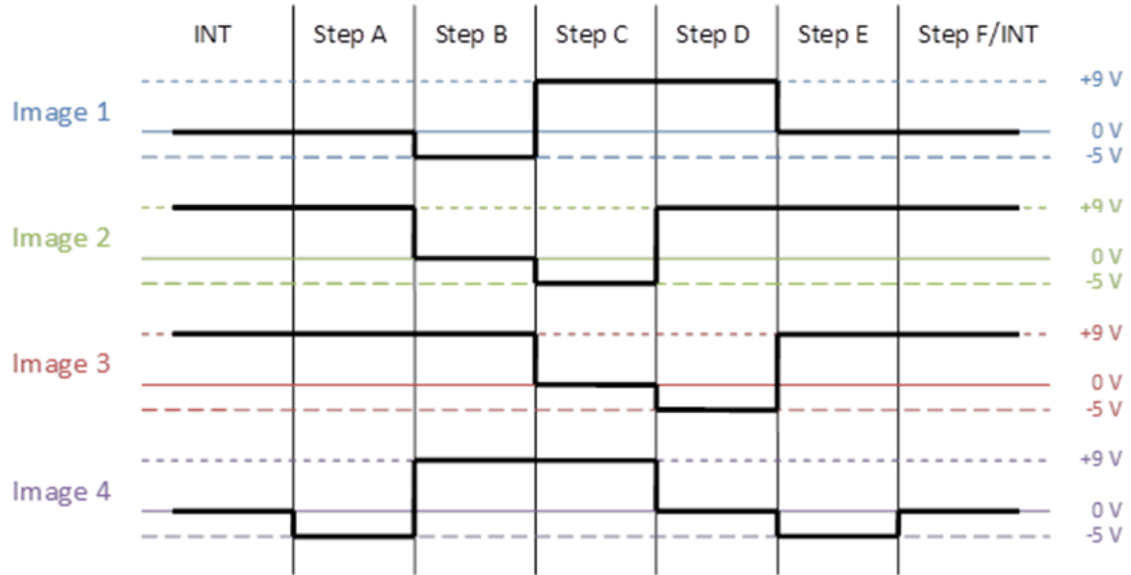


Figure 1. Example of a multiple (three) level parallel clocking scheme.

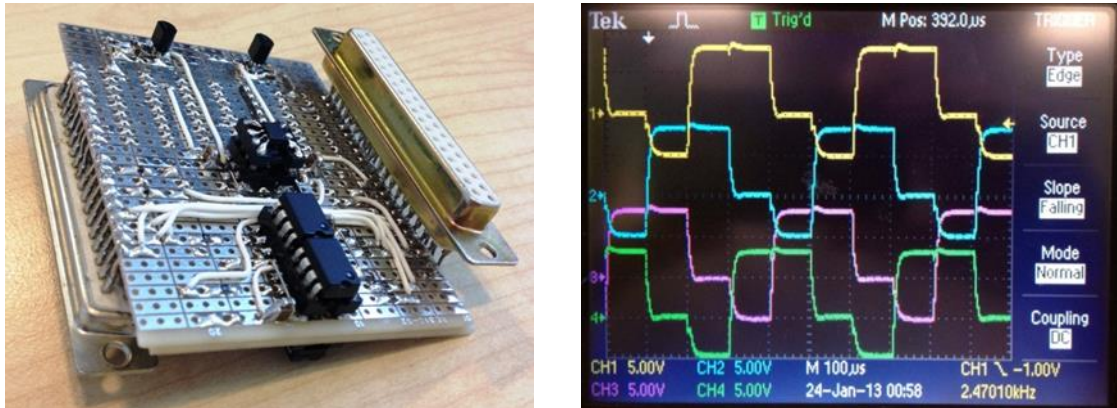


Figure 2. Left: High speed differential amplifier adapter circuit. Right: Load parallel clock waveforms.

3. CHARGE TRANSFER IMPROVEMENT

From the CTE optimisation work in [3], it was found that traps located under the barrier phases of the charge transport channel were responsible for reductions in CTE. By including a negative barrier phase, the potential barrier creating the row isolation can be given a forward transfer gradient to promote the re-joining of any trapped charges with their original charge packet.

Figure 3 shows an example using the potential well model of how charges can become trapped and released back into their original charge packets during transfer for readout. In the first step, charge is collected and stored in the potential wells in the CCD array formed by the collecting phase electrodes 2 and 3. In the next step, the charge is transferred into phases 3 and 4. The potential gradient induced by the negative phase 1 means that if any charge was trapped under phase 2, after a sufficient period it will rejoin with its original charge packet. The same process is repeated for all subsequent transfers.

Figure 4 shows the improvement in CTE for a three-level clocking scheme.

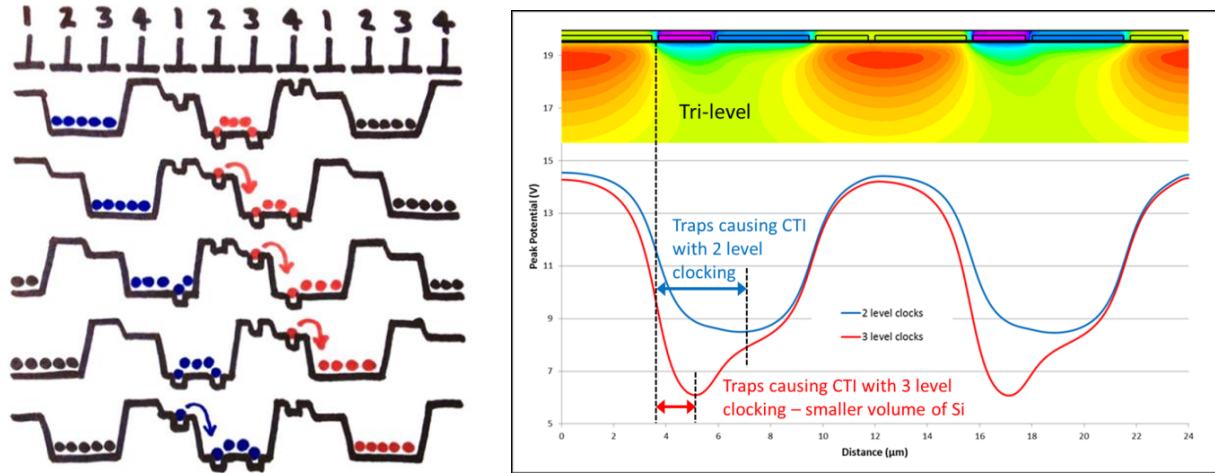


Figure 3. Left: Four-phase parallel forward clocking sequence using potential well model, showing how probability of charge being deferred by barrier phase traps can be reduced using multiple level clocks. Here each of the clock states is held for long enough that the trapped charge has likely been released. Right: Simulation of the potential well structure along the row direction of the CCD273 for the empty channel peak potential. The volume of silicon where traps in the transport channel may cause charge to be deferred is roughly halved by the used of three levels, indicated by the blue and red arrows.

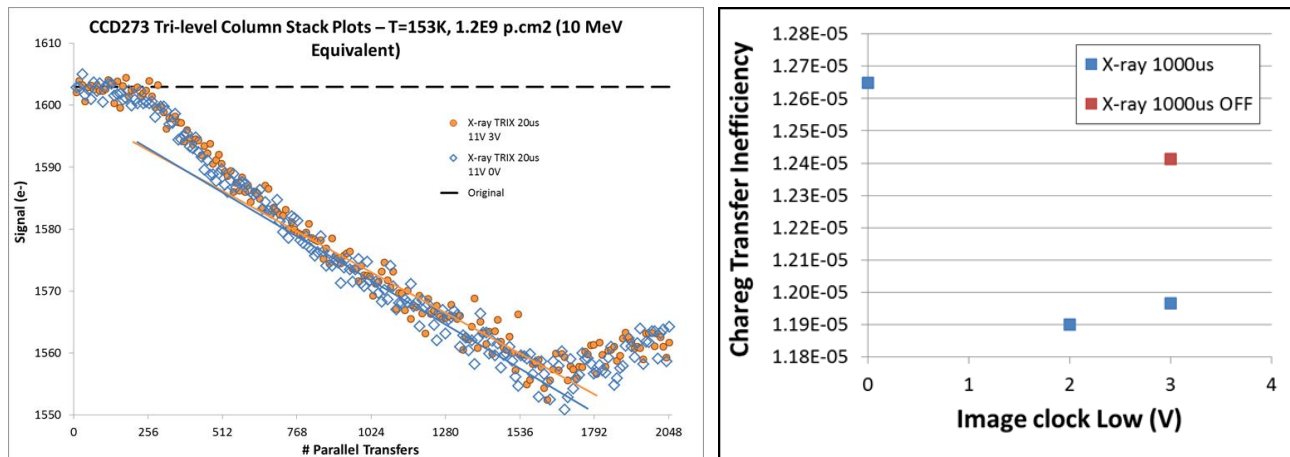


Figure 4. Left: X-ray column stack plots in CCD273 irradiated to 1.2E9 p.cm⁻² (10 MeV equivalent). The first ~256 columns are signals sampled in an unirradiated region of the device. The next 1,600 rows/parallel transfers are within the irradiated region. The initial steeper gradient is a consequence of ‘slow’ traps evenly distributed throughout the area; however the probability of encountering these is a function of the X-ray density in the area and reduced towards the beginning rows/transfers. The ‘settled’ gradient, indicated by the orange and blue lines is used to determine the ‘fast’ trap charge transfer inefficiency, shown right.

4. SURFACE PERSISTENCE CLEARING

During optical overload (blooming), or at any time where all clocks in the array are at a low state, charge may come into contact with Si/SiO₂ interface traps and become captured. This is when the device is operated with Image High ($I\bar{O}H$) \geq the channel parameter *i.e.* the Surface Full Well (SFW) regime. Where $I\bar{O}H <$ the channel parameter, the Bloomed Full Well (BFW) regime, surface persistence is not observed. Examples of these regimes are shown in Figure 5 (left).

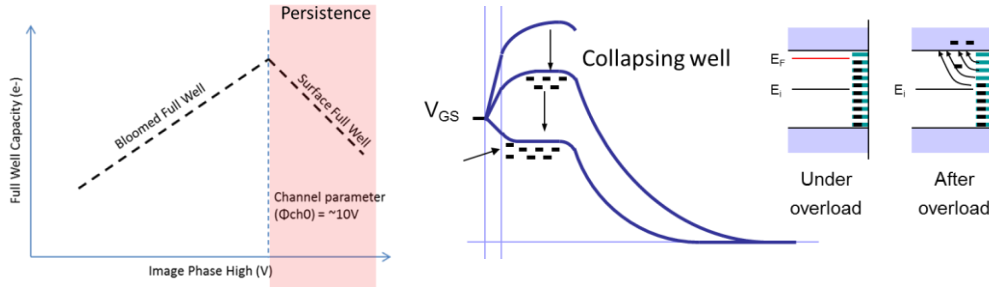


Figure 5. Left: Example of CCD full well regimes as a function of electrode bias. At $I\bar{O}H >$ the channel parameter, at the point of full well capacity, charge may come into contact with traps at the Si/SiO₂ interface. Right: Example of stored charge coming into contact and filling surface traps during optical overload.

Surface traps exist at continuum of energy levels across the band-gap as shown in Figure 5 (right) and hence exhibit multiple release time constants. Therefore, charge may then be released in later rows (not exhibiting exponential decay), manifesting as bright tails on signal, or subsequent long frame integrations, resulting in regions of localised increased background signal. This excess signal, persistence, will most likely be detrimental to performance in most astronomical applications.

Trapped charge can be removed with pinning by momentarily flooding the surface with holes that will recombine with any such electrons. Two schemes are available to achieve this: firstly the substrate potential can be raised between consecutive frames to a level approximately greater than +4 V and an example of this is shown in Figure 6. However, when using high resistivity devices with large negative substrate bias, raising it to such a level is unlikely to be practical. In addition this scheme does not mitigate the bright tailing observed in some images arising from the shorter time constant surface traps.

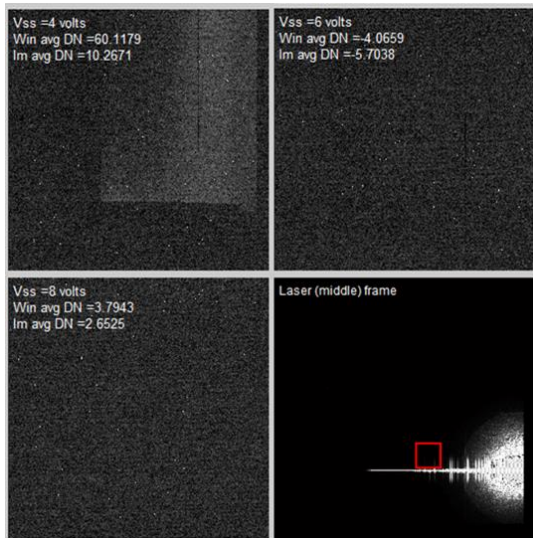
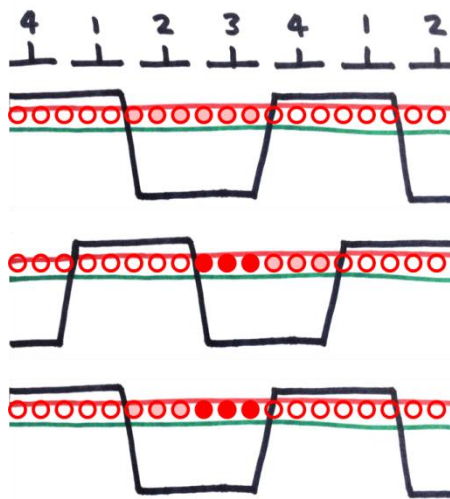


Figure 6. Example of raising the substrate between frames to clear surface persistence. The bottom right section shows a quadrant of the CCD273 over-exposed by a laser diode for 3 seconds. The remaining three sections show the residual signal collected in 300 second integrations, following the readout of the over-exposed frame. In each case the substrate was raised to +4 V, +6 V and +8V between frames. At +4 V, residual charge is still observed, however there is none at $> 6V$.

The second scheme available to pin the surface is to reduce the clock low level to a negative potential, typically -4 V or lower. Here all barrier phases are inverted in turn during the charge transfer sequence, providing holes to the surface interface states and recombining any trapped electrons during the clocking sequence. It may be possible that such a scheme will introduce measurable Clock-Induced-Charge (CIC), so careful consideration might be needed in the rise and fall of the parallel clock edges, exact biasing levels and using a fourth level to reduce the electric field strength.

5. CLOCKED ANTI-BLOOMING

When the silicon surface under an electrode is taken out of inversion, the return to normal levels of dark current is not immediate but builds up slowly with time as traps start refilling from the lowest energy levels upwards to the mid-band. The dark signal reverts to the normal level once the mid-band traps are filled. This phenomenon can be exploited to give lower levels of dark current in non-inverted mode devices by pulsing electrodes to shift the collection back and forth between two (or more) phases such that these are periodically inverted – dither mode clocking. The mean dark current is then dependent on the switching interval and device temperature. This method can also be used to ‘mop up’ excess charge that is trapped by the surface traps during optical overload – Clocked Anti-Blooming (CAB). Again, CIC can be a concern and so care must be taken over the clock amplitudes and timings.



Using potential well model, charge is collected under phases 2 and 3. As the well capacity is exceeded (green line), charge comes into contact with the surface (red line) and the surface traps (red o) begin to fill with excess charge. There are tens of thousands of surface traps per pixel. Before all surface traps are filled, the pixel is clocked forward by one electrode. Phase 2 is now pinned by taking it negative and the trapped charge is annihilated. Surface traps under phase 4 begin to fill with excess charge and the pixel is clock backwards by one electrode to the original position. Phase 4 is now pinned by taking it negative and the trapped charge is annihilated. Now surface traps under phase 2 begin to fill with excess charge again. This process is repeated many times during the frame integration.

Figure 7. Example of a Clocked Anti-Blooming scheme.

There are two well know problems associated with CAB. The first is the generation of CIC from the avalanche of holes in the high electric field created between the positive and negative electrodes. The second is trap pumping due to the dithering over pixel boundaries. Examples of both are shown in Figure 8.

For CAB to be useful in astronomical applications, a scheme needs to be developed to avoid both of these issues.

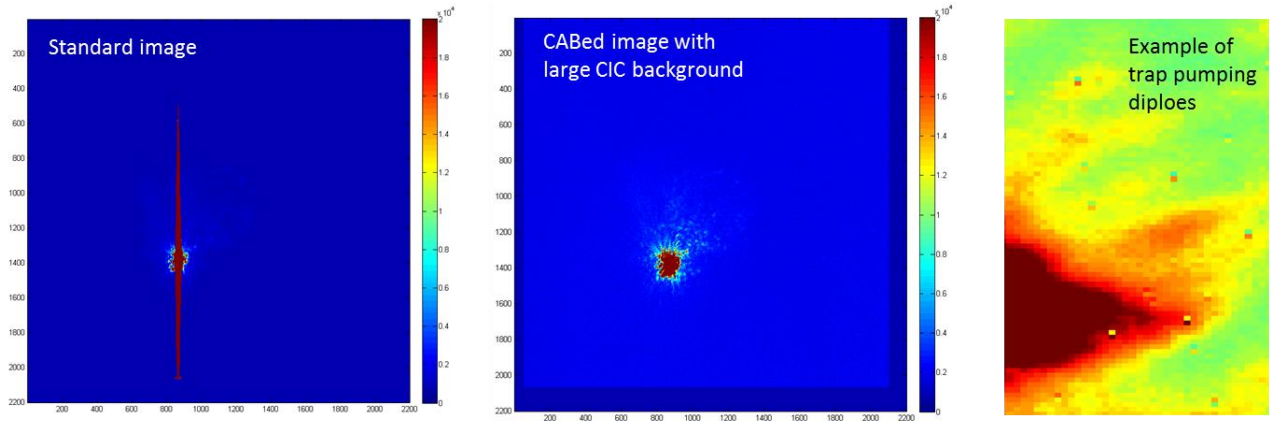


Figure 8. Left: Typical blooming observed during optical overload. Centre: Clock Anti-Bloomed image of the same exposure as before. Here there is no bloomed charge in the image, however an increased background generated by CIC. Right: Examples of trap pumped dipoles generated in the image areas containing sufficient background to be ‘pumped’.

In modern four-phase CCD architectures, we can use multiple-level clocking to reduce the electric field strength that holes may travel through and hence reduce the probability of generating CIC. Also from an increased understanding of the trap pumping process, we can avoid pumping traps during CAB by not dithering beyond the pixel boundary.

6. CLOCK INDUCED CHARGE

In the pinned state, some of the holes fill the surface traps and as the electrode is taken out of pinning the free holes move away to the less-positive areas. The trapped holes are then released over time but can multiply through impact ionisation while moving through the high electric field at the surface between the electrodes as shown in Figure 9. The resulting generation of electrons is termed Clock-Induced-Charge (CIC). The rate of generation is relatively low, but the number of collected electrons is cumulative with the number of transfers, or CAB cycles and exponentially dependent on the electric field strength and hence clock amplitudes.

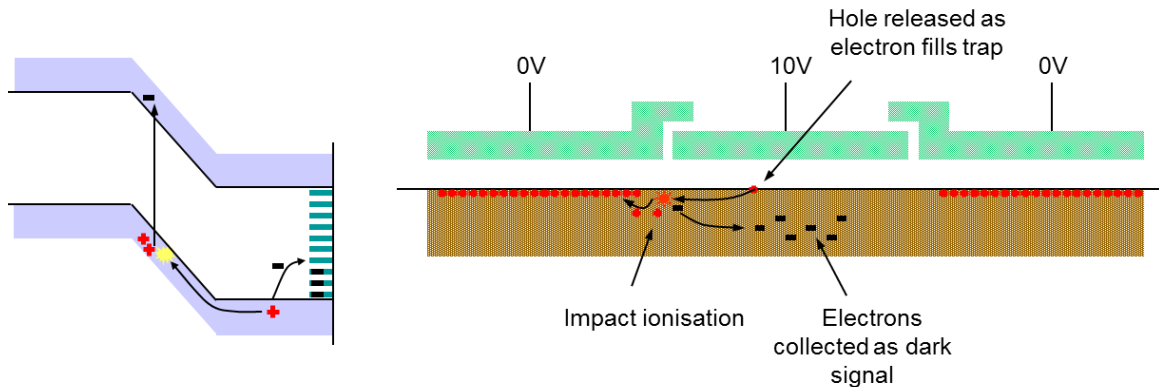


Figure 9. Example of the generation of CIC. Left: Energy band diagram of adjacent electrodes. Right: Physical location of holes generating signal electrons through impact ionisation at the electrode boundaries.

The use of multiple level clocking can be used to investigate the levels of CIC generated for a given sequence. Figure 10 demonstrates the amount of CIC generated for three examples of multiple level clocking. It is shown that quad-level clocking offers the least amount of CIC generation and so it was used to develop a CAB scheme.

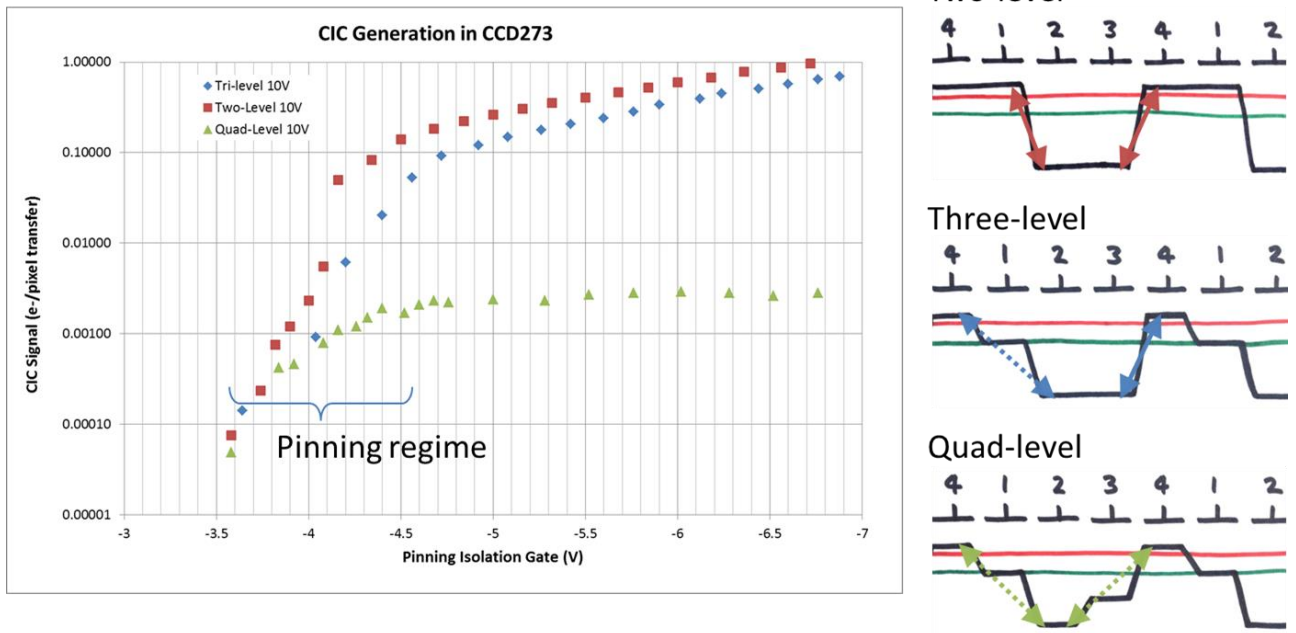


Figure 10. Measured CIC in CCD273 as a function of both clock amplitudes and electrode configuration. With two-level clocking, holes can generate electrons through impact ionisation in either direction of the row and so the maximum amount of CIC is measured. With three level clocking, the electric field strength is significantly reduced in one direction of the row and so the measured CIC is halved.

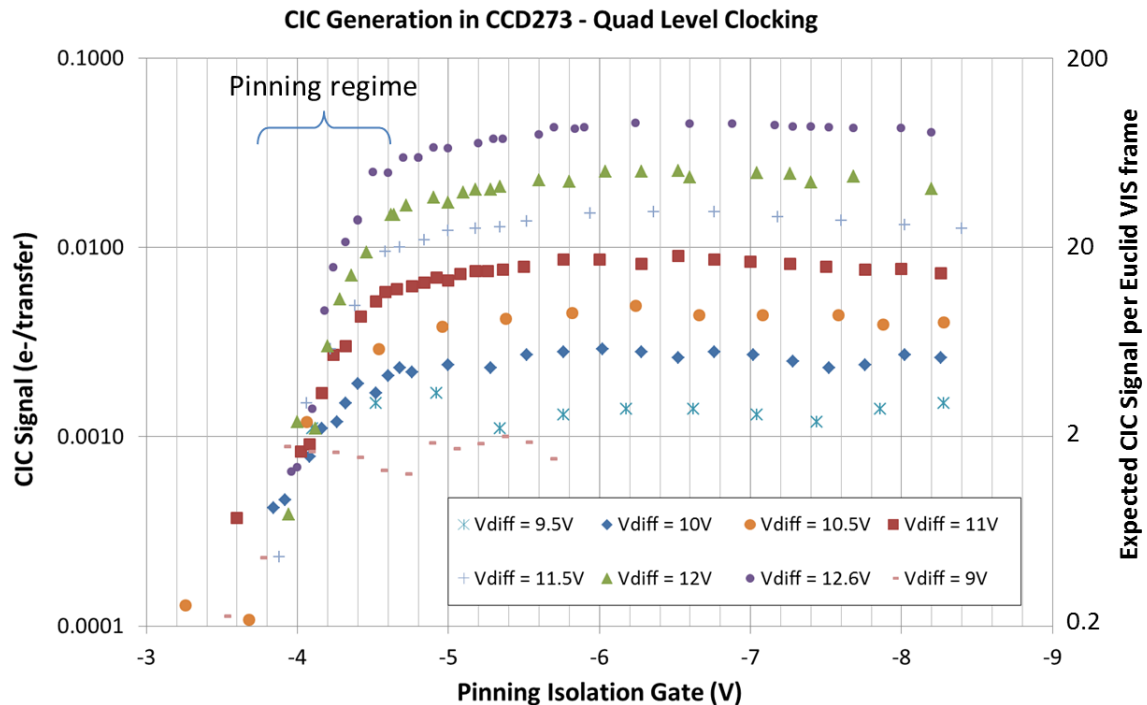


Figure 11. Measured CIC charge as a function of electric field strength with quad-level clocking. The level at which the CIC generation plateaus can be used to determine the suitable operation point for a given application.

7. QUAD-LEVEL PARALLEL CLOCKING SEQUENCE

Figure 12 show an example potential well model for a quad-level parallel clocking scheme that can be dithered by one electrode phase during integration to effectively anti-bloom without pumping traps, or generating CIC. As we want to be operating in the surface full well regime to make use of as many surface traps as possible for CAB, the image clock high level must be greater than +10 V and therefore +10.5 V is used. From Figure 11, we can also see that to fully pin the surface, the isolation gate needs to ~ -5 V. The fourth level reduces the electric field strength between clock high level and the pinned gate and is set by the differential amplifiers to $10.5 \text{ V} - 5 \text{ V} = 5.5 \text{ V}$.

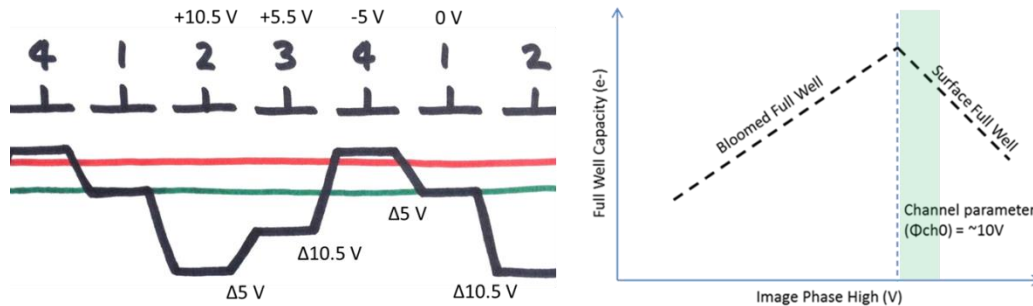


Figure 12. Left: Example potential well model. Right: Surface full well regime in typical CCDs.

A 660 nm laser diode was incident on the central region of a CCD273, generating signal at a rate of approximately 170 ke-/pixel/sec. Figure 13 (left) shows charge blooming observed without the use of the CAB scheme. In this example, some of the excess charge is being drained into the central charge injection structure and so a small region of parallel overscan is visible to the bottom of the image. In Figure 13 (right), CAB is employed at a rate of 40 μ s per cycle and no charge blooming is observed. Less than 4 electrons of CIC is generated per frame; however, this could be further reduced, or increased, depending on the anti-blooming rate required for the application. There is also no pumping of traps when using this CAB scheme.

The same quad-level parallel clock scheme and levels are used to transfer charge during readout to eliminate any surface persistence and improve CTE.

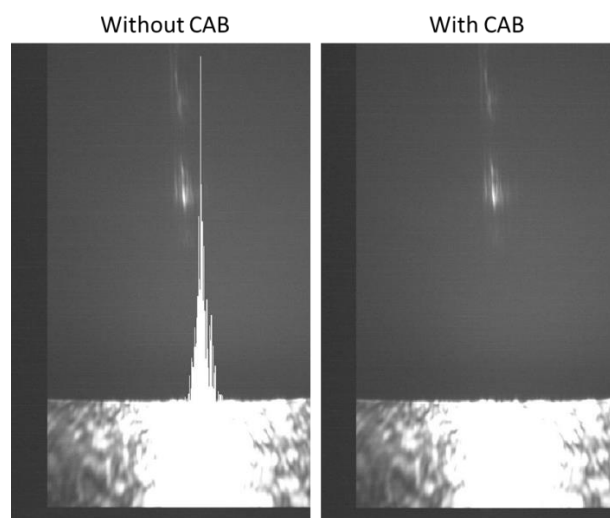


Figure 13. Results of the quad-level clocked anti-blooming scheme.

8. CIC BACKGROUND GENERATION

Figure 8 showed that CIC can generate a pretty uniform, but noisy background in the CCD. This CIC background can be manipulated in the CCD array to an advantage to inject backgrounds for any signal size, as the level of CIC is dependent on the number of clocking cycles and the field strength. Figure 14 shows examples of CIC background generated with various numbers of parallel forward transfers occurring during the CIC generation. These forward transfers are used to average the fixed noise pattern component of the CIC background arising from the physical geometries of each pixel.

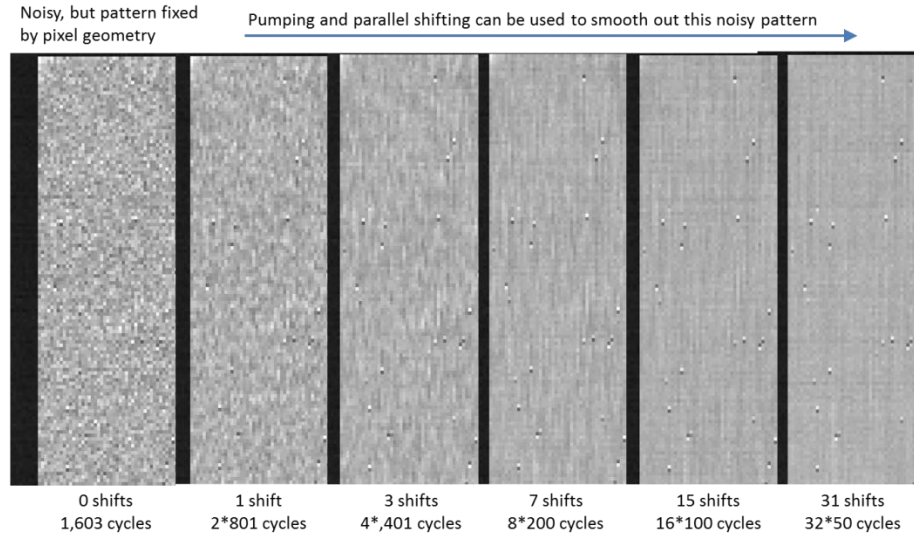


Figure 14. Examples of background generation using CIC with trap pumping performed as a separate step afterwards.

9. CONCLUSIONS

The number of barrier phase traps degrading charge transfer efficiency can be reduced by altering the potential structure between row pixels with a multi-level clocking scheme. This is desirable in astronomical applications where the very best charge transfer efficiency is required. A multi-level readout clocking scheme, if sufficiently negative, will pin the entire surface of the device during a single row transfer – this will clear any surface persistence/memory effects between frames. In long exposures, such as Euclid VIS (565 seconds) it is absolutely necessary that persistence is avoided. Clocked Anti-Blooming was shown to work in 4-phase CCDs, without generating CIC or pumping traps. Bloomed signal is most undesirable as it reduces the science return from a frame. CIC generation can be manipulated to provide uniform charge injection into the device. This could be used as part of an on-orbit calibration scheme, where single-electron traps are routinely pumped. Not only could such a scheme be useful for Euclid VIS, but we can also further manipulate the injected signal for FPR and EPER measurements. A single set of operating conditions can be found to allow all these features in a single camera setup

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